

⑪ Ⓐ **No.** 1006568

④⑤ **ISSUED** 770308

⑤② **CLASS** 313-63  
**C.R. CL.** 352-54

①⑨ Ⓐ

# CANADIAN PATENT

⑤④ **ELECTRONIC STORAGE TUBE**

⑦⑦ **Hofstein, Steven R.,**  
**U.S.A.**

**Granted to Princeton Electronic Products, Inc.,**  
**U.S.A.**

②① **APPLICATION No.** 069,407

②② **FILED** 691209

③⑦ **PRIORITY DATE** U.S.A. (840,698) 690710

**No. OF CLAIMS** 11

ABSTRACT OF THE DISCLOSURE

An electronic storage tube having a target whose conducting areas are silicon and whose insulating areas are silicon dioxide. One configuration of the target is a pattern of alternating strips of conducting areas and insulating areas.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. An electronic storage tube including a target which is comprised of a pattern of a plurality of alternating insulating and conducting stripe areas, the tube comprising:  
5 means for applying a signal to the target to establish a desired stored charge distribution on the insulating areas; and means for detecting the stored charge distribution established on the target; and wherein  
the conducting areas are electrically connected to each other and are formed of silicon; and  
10 the insulating areas are formed of silicon dioxide.
2. The invention of Claim 1 including a conducting substrate silicon and insulating areas overlying the conducting substrate such that the pattern of conducting and insulating areas is formed thereby.
3. The invention of Claim 2 wherein the pattern comprises a plurality of discrete areas.
4. The invention of Claim 1 including an insulating substrate and a conducting layer overlying the insulating substrate; the conducting layer having openings therein such that the pattern of conducting and insulating areas is formed thereby.
5. The invention of Claim 1 or Claim 2 wherein the insulating areas are genetically derived from the conducting areas.
6. The invention of Claim 3 or Claim 4 wherein the insulating areas are genetically derived from the conducting areas.

# 1006568

7. An electron storage device having information storage capabilities, comprising an evacuated envelope, a storage target disposed within said envelope comprising a body having a plurality of semi-conducting regions and storage regions alternating across a major surface of said body, said storage regions covering a portion of said major surface and having the configuration of substantially parallel strips, said semi-conducting regions consisting of semi-conductor material of a substantially single conductivity type, said storage regions consisting essentially of an insulating compound of a semiconductor material, and means for writing information on said storage target, for reading said information, and for erasing said information.

8. The electron storage device defined in Claim 7, wherein said semi-conductor material is silicon and said insulating compound is silicon dioxide.

9. An electronic storage tube comprising:

a target having a pattern of alternating stripes of conducting areas and insulating areas; an output terminal; the conducting areas being formed of silicon and being electrically connected to the output terminal; the insulating areas being formed of silicon dioxide; means for applying an input signal to the target such that a signal is stored thereon in the form of a desired stored charge distribution on the insulating areas; means for scanning the target and obtaining an output signal at the output terminal which output signal is a function of the stored charge distribution on the insulating areas.

10. The invention of Claim 9 wherein the insulating areas are genetically derived.

11. An electron storage device comprising an evacuated envelope, a storage target electrode mounted within the envelope and including an electrically conductive substrate and a layer of electrically insulating material on one surface of said substrate, said substrate having apertures extending there-  
5 through to said one surface of said substrate, said insulating layer having electrically insulating storage regions adjacent to said apertures and capacitively coupled to said substrate, a first means for establishing a negative charge pattern relative  
10 to a reference potential on said storage regions and a positive potential relative to said reference potential on said conductive substrate, a second means for directing and scanning an unmodulated electron beam over the surface of said charged insulating layer, said second means including an electron gun having a cathode  
15 operated at said reference potential whereby electrons from said beam are deflected by the negative charge pattern on said insulating layer to said substrate, said substrate being formed of P or N type silicon, and said storage regions being silicon dioxide formed from the material of the substrate.

This invention relates to electronic storage tubes. In particular, it relates to certain target configurations and target composition.

Broadly, electronic storage tubes are comprised of a target for storing information of a writing signal, means for directing the writing signal (generally an electron beam) onto the target and means for reading the stored information at an output terminal. Usually, targets of electronic storage tubes are made of a conducting mesh covered with a thin insulating film or of a continuous di-electric film with an overlay of  
10 a conductive mesh material.

Thus, the invention contemplates an electronic storage tube including a target which is comprised of a pattern of a plurality of alternating insulating and conducting stripe areas. The tube comprises means for applying a signal to the target to establish a desired stored charge distribution on the insulating areas, and means for detecting the stored charge distribution established on the target. The conducting areas are electrically connected to each other and are formed of silicon and the insulating areas are formed of silicon dioxide.  
20

It is an important object of the invention to provide an electronic storage tube wherein the target is formed of alternating conducting areas and insulating areas and wherein the conducting areas are formed of silicon and the insulating areas are formed of silicon dioxide.

It is another important object of the invention to provide a target for an electronic storage tube as described above wherein the target is formed of alternating stripes of conducting areas and insulating areas and the scanning directions of the writing beam and reading beam across the target are transverse  
30 to the longitudinal dimension of the stripes.

It is a further object of the invention to provide a target

of silicon and silicon dioxide wherein the silicon dioxide is genetically derived from the silicon.

These and other objects, advantages, features and uses will be apparent during the course of the following description when taken in conjunction with the accompanying drawings wherein:

FIGURE 1 is a diagrammatic, elevational view of an electron storage tube utilizing the targets of the invention;

FIGURE 2 is a plan view of a target of the invention wherein the pattern is comprised of alternating stripes of conducting areas and insulating areas;

FIGURE 3 is a sectional view taken along the lines 3-3 of FIGURE 2, viewed in the direction of the arrows;

FIGURE 4 is a sectional view illustrating the steps of a preferred method for producing targets of the invention;

FIGURE 5 is a plan view of another embodiment of target of the invention;

FIGURE 6 is a sectional view taken along the lines 6-6 of FIGURE 5, viewed in the direction of the arrows;

FIGURE 7 is a view similar to that of FIGURE 6 of a further embodiment of the target of the invention; and

FIGURE 8 is a view similar to that of FIGURE 6 of a still further embodiment of the target of the invention.

In the drawings, wherein, for the purpose of illustration, there are shown various embodiments of the invention, the numeral 10 designates an electronic storage tube of the invention, generally Storage tube 10 is seen to comprise (FIGURE 1) envelope 12, control grid 14, cathode 16, accelerating anode 18, wall anode 20, target 22 which comprises substrate 24 and mosaic layer 26, deflecting coil 28, focusing coil 30, output terminal 32 and grid mesh 34.

The Write signal is applied to the target by either x-y deflection of the electron beam emitted by the cathode 16 or by z-axis modulation of a raster scanned beam. The Read signal is a normal raster scan electron beam which is applied to the target. During the Read cycle, output current proportional to the charge pattern on the target (the distribution of charge on the insulating areas of the target) is obtained at output terminal 32 when the normal raster scan electron beam sweeps the target 22.

10 During the Read cycle, the insulating mosaic of the target acts essentially as a coplanar grid so that the more negative the potential on the insulating areas is, the lower the current on the conducting areas. It is possible to completely cut off the current to the conducting areas by placing a sufficiently high negative potential on the insulating areas.

To Erase the stored signal, it is necessary to re-establish a uniform charge pattern on the insulating mosaic. This charge pattern may be positive, negative or zero depending on the requirement of the Write mode. For the high velocity Write mode described above, a uniform high, negative charge is required to be left on the insulating mosaic after the Erase mode is completed. If "Equilibrium" or "low velocity" Write signals are used, a zero or slightly negative charge should remain on the insulating mosaic after the Erase mode is completed.

20

In FIGURES 2 and 3 there is illustrated a preferred embodiment of target which may be employed in practising the invention. Target 40 comprises conducting substrate 42 and insulating stripes 44. The conducting substrate 42 is silicon. The silicon may be of the P-type or N-type. The insulating stripes are preferably formed of silicon dioxide.



# 1006568

Targets, which are formed with the pattern of alternating insulating stripes and conducting stripes have some advantage over other target mosaic configurations such as are illustrated in FIGURES 5-8. Where the pattern of target 50 is formed, as is illustrated in FIGURES 5 and 6, with a mosaic of insulating pads 54 on a conducting substrate 52, certain limitations in operation exist.

The exposed conducting areas 52 actually comprise a crossed grid of both vertical and horizontal stripes. This crossed or  
10 double grid increases the possibility of failure due to insulator cross-overs or insulator gaps. Furthermore, both the horizontal and vertical resolution are determined by the structure of the target, namely, the vertical and horizontal spacing dimensions.

To obtain maximum resolution from the configuration of FIGURES 5 and 6, the horizontal dimensions A and B of both the conducting and insulating areas should be minimized. If the minimum dimension consistent with edge resolution is defined as C, then  
20  $A=C$  and  $B=C$  or  $A=B=C$ . However, then the ratio of conducting area to insulating area is 3:1 which is not ideal for information storage. This disparity between the conducting area and the insulating area results in non-uniform, relatively poor control of the Read electron beam by the stored-charge image.

In the improved structure of FIGURES 2 and 3, the widths of the insulating stripes 44 and the conducting stripes 43 are approximately equal. With this striped configuration, the dimensions may be made equal and minimized for maximum resolution while maintaining the area ratio at 1:1. This ratio is optimum for satisfactory control of the Read beam. Moreover, because the electron beam traverses the target in a direction transverse to

the longitudinal direction of the stripes, an additional advantage resides in the fact that resolution in the longitudinal direction of the stripes is no longer limited by the target structure, resulting in higher resolution capability. Since this construction is a "single" grid, only one "failure" or "bridging" mode is possible, namely, that across the stripes.

It is preferable to form the target of FIGURES 2 and 3 of doped silicon and silicon dioxide. The conducting areas are formed of the doped silicon, either P or N, and the insulating areas are formed of the silicon dioxide. Excellent targets of the type described are obtained when the silicon dioxide layer is genetically derived from the silicon. A genetically derived layer is one in which the insulating layer is derived from the conducting base or substrate material. This can be accomplished, for example, by immersing the silicon in a chemical solution such as N-Methyl-Acetamide or similar materials while applying a voltage to the silicon (anodically grown). Other methods of genetically deriving the insulating layer may also be used.

A preferred process for forming a genetically derived target of the invention is illustrated in FIGURE 4. A silicon wafer of doped silicon is specially cleaned with a suitable solvent to eliminate all surface imperfections and contaminants. It is then oxidized at temperatures of the order of 1100°C-1250°C so that a high quality silicon dioxide layer 62 is formed on silicon substrate 60. Layer 62 is about 1 micron thick.

The silicon dioxide surface is coated with a photosensitive lacquer 64. The unit is exposed to light through an optical mask of the desired pattern and then developed. The exposed portions of silicon dioxide layer 62 are then removed by dilute hydrofluoric

acid and the photoresist 64 is stripped from the surfaces of the stripes of silicon dioxide. This leaves a substrate of conducting silicon with a mosaic layer of insulating silicon dioxide. In the stripe configuration of FIGURES 2 and 3, the width of each of the stripes 43 is of the order of 3-7 microns.

It is also within the contemplation of the invention to form targets of silicon and silicon dioxide which have the pattern illustrated in FIGURES 5 and 6.

10 In FIGURE 7 there is illustrated a target wherein the substrate 70 is conductive and the insulator film 72 is provided with holes 73 so that the desired pattern of substrate 70 is exposed to the electron beam.

In FIGURE 8, substrate 74 is an insulator and conductive film 76 is provided with holes 77 so that the desired pattern of substrate 74 is exposed to the electron beam.

The embodiment of FIGURES 7 and 8 may be used with the particular patterns illustrated in FIGURES 2 and 5 or with any other desired pattern.

20 The desired target of one of the types described is installed in electron tube 10 which is produced in any manner which is well-known in the art. By way of illustration, operation of electronic storage tubes of the invention may then proceed as follows:

To Write, target 22 is placed at about +250 volts and grid 14 is kept at approximately -60 volts. The information to be stored is placed on grid 14 with a peak-to-peak signal of approximately 10 volts. Under these conditions the information can be written in about 1/30th of a second (1 TV frame).

For read-out, the target is returned to about +8 volts. It is scanned in conventional raster format with the voltage on

grid 14 adjusted to yield an output signal at terminal 32 of approximately 200 nA. Continuous read-out is possible under the above conditions for more than 10 minutes. Longer storage time is possible if the read-out signals are smaller. Because of the dielectric relaxation time of silicon dioxide, with the beam off, the storage time will be a week or more.

The storage signal on the target can be erased by applying about +20 volts to target 22, setting grid 14 at approximately zero volts to yield maximum beam current and scanning the area to be erased. Now, the erased area is ready to accept new information without the necessity for a prime cycle.

During the Write cycle the target voltage is about +250 volts. At this voltage, the electrons from the beam which impinge on the silicon dioxide layer 26 cause secondary emission of the order of 5:1 and the net electron current to the silicon dioxide is negative. At increased target voltage, the secondary emission ratio decreases because secondary electrons are formed deep in the silicon dioxide and have difficulty escaping. The Write cycle is performed in the flat portion of the curve which plots electronic current to the silicon dioxide against target voltage, namely, about +250 volts. There is another flat portion of the curve at about 1000 to 2000 volts.

The Write cycle is carried on at the flat region of the curve so that the surface of the silicon dioxide is charged positively. This positive charge is proportional to the number of electrons impinging on that area of the target. This yields a positive, linear relationship between the electron current from the gun and the positive charge on the target.

During the Read cycle, the silicon (conducting portion)

plate or substrate 24 is returned to a potential which sets the insulating portion 26 negative with respect to cathode 16. The regions that are very negative prevent any current flow to the silicon (corresponding to a "black" picture). The regions which are only slightly negative will allow a significant current flow to the silicon (corresponding to a "white" picture). Since the signal from the target may be inverted electrically, if desired, the very negative regions (no current flow) may correspond to a "white" signal and the slightly negative regions (significant current flow) may correspond to a "black" signal.

10

The Erase cycle simply charges the surface of the insulating areas to a uniformly negative value so that no electronic current can flow to the conducting substrate because of the repulsion effect of the coplanar insulating grid.

While particular embodiments and examples of the invention have been shown and described, it will be apparent to those skilled in the art that modifications are possible without departing from the spirit and scope of the invention.

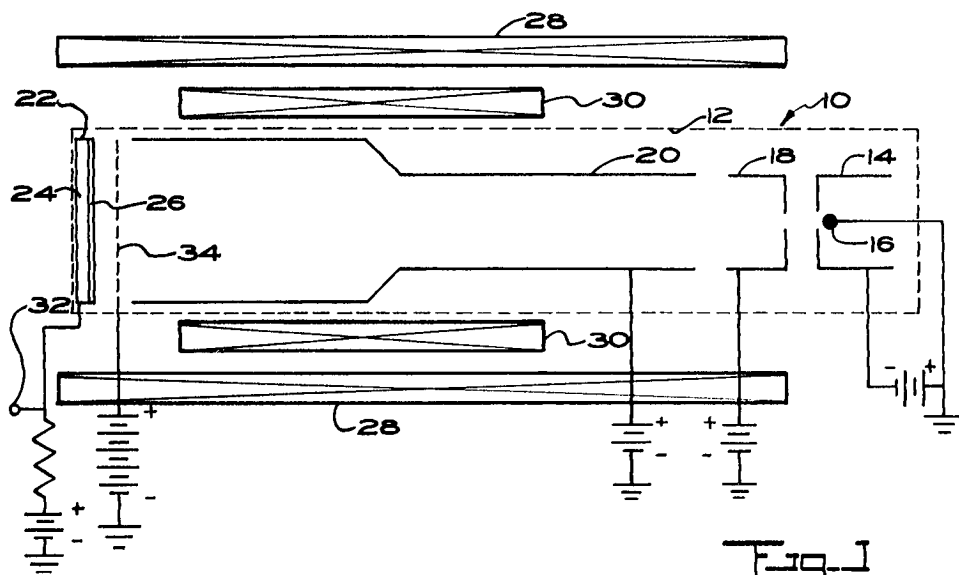


Fig. 1

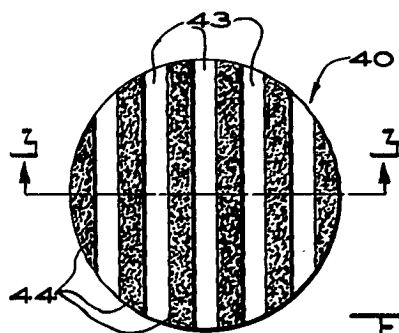


Fig. 2

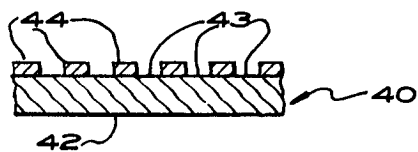


Fig. 3

INVENTOR  
STEVEN R. HOFSTEIN

*Samuelson & Jacob*

PATENT AGENT

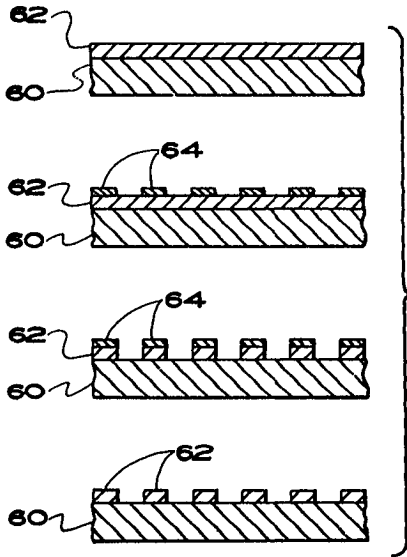


Fig 4

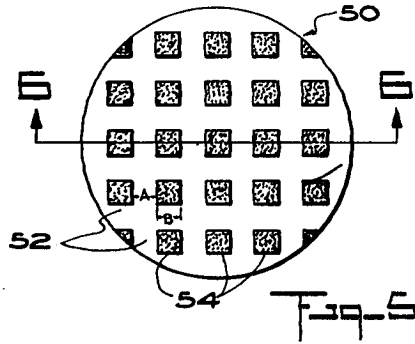


Fig-5

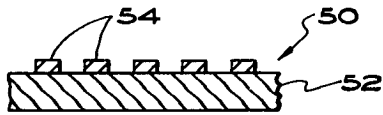


Fig-6

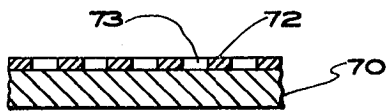


Fig-7

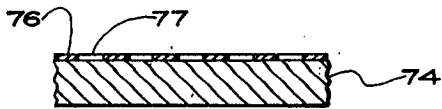


Fig-8

INVENTOR  
STEVEN R. HOFSTEIN

*Shumelton & Jacob*

PATENT AGENT